Remarks

The Office Action mailed January 7, 2005 has been received and reviewed. Claims 57, 60, 63, and 66 having been amended, and claims 69-74 having been added, the pending claims are claims 45-74.

Claims 57 and 63 have been amended to recite that the opening has an aspect ratio greater than about 1, which is supported, for example, by claims 60 and 66, respectively. Claims 60 and 66 have been amended to recite an aspect ratio of greater than about 3, which is supported by the specification at, for example, page 16, line 5.

New claims 69-74 are generally supported, for example, by claims 57-62. New claims 69-74 further recite the proviso that the surface defining the opening is not a silicon containing surface. The recitation of the proviso that the surface defining the opening is not a silicon containing surface is supported by the positive recitation of a silicon containing surface in the specification at, for example, page 3, line 26 to page 4, line 2. See, for example, M.P.E.P. §2173.05(i), which states that "[i]f alternative elements are positively recited in the specification, they may be explicitly excluded in the claims." Applicants respectfully submit that the specification recites alternative surfaces for substrate assemblies (e.g., page 7, lines 12-20) including surfaces that are silicon containing materials, as well as one or more layers formed thereon (e.g., non-silicon containing conductive layers as recited in the specification at, for example, page 13, lines 19-25). Thus, Applicants respectfully submit that no new matter has been added.

Reconsideration and withdrawal of the rejections are respectfully requested.

Rejections under 35 U.S.C. §102

Matsubara et al.

The Examiner rejected claims 45-48, 50, and 51 under 35 U.S.C. §102(b) as being anticipated by Matsubara et al. (U.S. Patent No. 5,122,923). Applicants respectfully traverse the rejection.

Independent claims 45 and 50 each recite a chemical vapor codeposited diffusion barrier layer formed of $RuSi_x$, where x is in the range of about 0.01 to about 10. Applicants respectfully submit that Matsubara et al. fail to disclose or suggest such a chemical vapor codeposited diffusion barrier layer formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

In contrast, Matsubara et al. disclose a sputtering technique to form a lower electrode layer of $RuSi_2$. It is the Examiner's position that " 'chemical vapor codeposited' merely recites a method of forming and does not deviate from the **structure of a diffusion barrier made of $RuSi_x$**" (page 6, lines 3-4 of the Office Action mailed January 7, 2005; emphasis in original). Applicants respectfully disagree.

In the Amendment and Response submitted October 4, 2004, Applicants argued that a diffusion barrier layer formed using chemical vapor deposition as recited in the present invention is different than the layer sputtered according to Matsubara et al., the arguments of which are hereby incorporated by reference.

In response, the Examiner acknowledged Applicants' arguments, but asserted that the claims do not state any of the structural differences. Applicants earnestly disagree. Applicants resepectfully submit that those skilled in the art would appreciate that the term "chemical vapor deposited" when used to define a layer describes a structurally different layer than when the term "sputtered" is used to define a layer. As such, the term "chemical vapor codeposited" is not merely a product-by-process limitation and must be given patentable weight in the pending claims.

Moreover, Applicants submitted a "Declaration Under 37 C.F.R. §1.132" signed by the inventors (filed in response to the Final Office Action dated 25 November 2002) that stated, in part, "that sputter coated diffusion barrier layers and chemical vapor deposited diffusion barrier layers have different structures. As such if a chemical vapor deposited diffusion barrier layer and a sputter coated diffusion barrier layer were analyzed by one skilled in the art these structural differences . . . [e.g., conformality, coverage uniformity, pinhole count, stress control, and/or underlying surface damage] would allow one skilled in the art to identify the diffusion barrier layer as either being a sputter coated diffusion barrier layer or a diffusion barrier layer

having been deposited by a different technique (e.g., chemical vapor deposited diffusion barrier layer)" (item 14).

However, the Examiner is of the opinion that the Declaration has little probative value. Applicants earnestly disagree. For example, the Examiner asserted that "[s]ince Matsubara discloses a simple diffusion barrier layer 3 on a flat surface, it would be reasonable to assume that in such a simple structure, no surface damage would occur ***to the diffusion barrier layer*** (page 8, lines 4-6 of the Office Action mailed January 7, 2005; emphasis added). Applicants respectfully submit that the Examiner's conclusory assertion is totally unsupported by evidence in the Office Action, and, in fact, is not even commensurate with the statements made in the Declaration. Specifically, the Declaration states that ***an underlying substrate*** to a sputter coated diffusion barrier layer, not the ***diffusion barrier layer itself***, may have surface damage" (item 9). Further, the Declaration provides no suggestion that such surface damage would not occur for a simple diffusion barrier layer on a flat surface as asserted by the Examiner. In the event that the Examiner's assertion is not withdrawn in the next Official Communication, Applicants respectfully request that the Examiner provide proper support for his assertion.

For another example, the Examiner asserted that "Matsubara discloses (see, for example, FIG. 1) a silicon oxide layer 2 in between the substrate 1 and lower electrode 3. It is physically not possible that a metal such as ruthenium that is used to form the lower electrode 3 can implant into the substrate when there is a silicon oxide layer covering the substrate" (page 8, lines 7-10 of the Office Action mailed January 7, 2005; emphasis added). Applicants respectfully submit that the Examiner's conclusory assertion is totally unsupported by evidence in the Office Action, and, in fact, is not even commensurate with the statements made in the Declaration. Specifically, the Declaration states that that ***an underlying substrate***, not necessarily a ***silicon substrate***, to a sputter coated diffusion barrier layer may have surface damage that may include implantation of metal in the underlying substrate. Further, the Declaration provides no suggestion that such surface damage would not occur for a silicon oxide layer. In the event that the Examiner's assertion is not withdrawn in the next Official Communication, Applicants respectfully request that the Examiner provide proper support for his assertion.

Finally, the Examiner asserted that Applicants "provided no scientific evidence to support the statements in the Declaration" (page 7, lines 3-4 of the Office Action mailed January 7, 2005). Applicants respectfully submit that the Examiner has failed to specifically explain why Declarants' statement, that "if a chemical vapor deposited diffusion barrier layer and a sputter coated diffusion barrier layer were analyzed by one skilled in the art these structural differences, as described above, would allow one skilled in the art to identify the diffusion barrier layer as either being a sputter coated diffusion barrier layer or a diffusion barrier layer having been deposited by a different technique (e.g., chemical vapor deposited diffusion barrier layer)" (item 14), is insufficient to overcome the rejection.

Moreover, Applicants wish to draw the Examiner's attention to the following documents, which support the position that those skilled in the art would appreciate that the term "chemical vapor deposited" when used to define a layer describes a structurally different layer than when the term "sputtered" is used to define a layer. *See, for example*, Wolf et al., which is submitted concurrently herewith in an Information Disclosure Statement, stating that "CVD offers several advantages over other techniques for silicide formation including, improved step coverage, ***higher purity films (low O_2 content)***, and higher throughput" (page 392, last paragraph; emphasis added). Applicants respectfully submit that ***higher purity films (low O_2 content) is a structural property*** that could be analyzed by one of skill in the art, and moreover, that oxygen contamination in the silicide film also has a significant effect on the ***film resistivity*** (page 388, second paragraph), which is ***also a structural property*** that could be analyzed by one of skill in the art. For another example, Yao-Joe Yang states that "[s]ubstrate damage is the major disadvantage" of sputtering (page 5, slide 9; *see, also*, page 6, slide 11).

As such, the term "chemical vapor codeposited" is not merely a product-by-process limitation and must be given patentable weight in the pending claims. Reconsideration and withdrawal of the rejection of claims 45-48, 50, and 51 under 35 U.S.C. §102 as being anticipated by Matsubara et al.

Kuroiwa et al.

The Examiner rejected claims 45, 46, 50, and 51 under 35 U.S.C. §102(e) as being anticipated by Kuroiwa et al. (U.S. Patent No. 6,239,460). Applicants respectfully traverse the rejection.

Independent claims 45 and 50 each recite a chemical vapor codeposited diffusion barrier layer formed of $RuSi_x$, where x is in the range of about 0.01 to about 10. Applicants respectfully submit that Kuroiwa et al. fail to disclose or suggest such a chemical vapor codeposited diffusion barrier layer formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

In contrast, Kuroiwa et al. disclose the deposition of ruthenium on a silicon plug, followed by heat treatment to form a ruthenium silicide layer through a salicidation process. It is the Examiner's position that " 'chemical vapor codeposited' merely recites a method of forming and does not deviate from the **structure of a diffusion barrier made of $RuSi_x$**" (page 6, lines 3-4 of the Office Action mailed January 7, 2005; emphasis in original). Applicants respectfully disagree.

In the Amendment and Response submitted October 4, 2004, Applicants argued that a diffusion barrier layer formed using chemical vapor deposition as recited in the present invention is different than a layer formed by a salicidation process according to Kuroiwa et al., the arguments of which are hereby incorporated by reference.

In response, the Examiner acknowledged Applicants' arguments, but asserted that the claims do not state any of the structural differences. Applicants earnestly disagree. Applicants resepectfully submit that those skilled in the art would appreciate that the term "chemical vapor deposited" when used to define a layer describes a structurally different layer than a layer formed by a salicidation process. As such, the term "chemical vapor codeposited" is not merely a product-by-process limitation and must be given patentable weight in the pending claims.

Moreover, Applicants wish to draw the Examiner's attention to the following documents, which support the position that those skilled in the art would appreciate that the term "chemical vapor deposited" when used to define a layer describes a structurally different layer than a layer

formed by a salicidation process. *See, for example*, Wolf et al., which is submitted concurrently herewith in an Information Disclosure Statement, stating that "CVD offers several advantages over other techniques for silicide formation including, improved step coverage, ***higher purity films (low O_2 content)***, and higher throughput" (page 392, last paragraph; emphasis added). Applicants respectfully submit that ***higher purity films (low O_2 content) is a structural property*** that could be analyzed by one of skill in the art, and moreover, that oxygen contamination in the silicide film also has a significant effect on the ***film resistivity*** (page 388, second paragraph), which is ***also a structural property*** that could be analyzed by one of skill in the art.

As such, the term "chemical vapor codeposited" is not merely a product-by-process limitation and must be given patentable weight in the pending claims. Reconsideration and withdrawal of the rejection of claims 45, 46, 50, and 51 under 35 U.S.C. §102 as being anticipated by Kuroiwa et al.

Rejection under 35 U.S.C. §103

Kuroiwa et al. in view of Aoyama et al.

The Examiner rejected claims 48, 49, and 54-68 under 35 U.S.C. §103 as being unpatentable over Kuroiwa et al. (U.S. Patent No. 6,239,460) and further in view of Aoyama et al. (U.S. Patent No. 5,852,307). Applicants respectfully traverse the rejection.

Applicants respectfully submit that the cited documents do not teach or suggest all of the language recited in the present claims. Specifically, Kuroiwa et al., which has been discussed herein above, lacks, among other things, a chemical vapor codeposited $RuSi_x$ diffusion barrier layer. Applicants respectfully submit that Aoyama et al., which "relates to a semiconductor device, and in particular to a semiconductor device provided with a capacitor comprising a dielectric film made of a metal oxide, and to a method of manufacturing the semiconductor device" (column 1, lines 6-9), fails to cure the deficiencies of Kuroiwa et al. Thus, for at least this reason, Applicants respectfully submit that claims 48, 49, and 54-68 are patentable over Kuroiwa et al. in view of Aoyama et al.

Further, independent claims 57 and 63 each recite a surface defining an opening having an aspect ratio greater than about 1, and a chemical vapor codeposited diffusion barrier layer over at least a portion of the surface defining the opening.

The Examiner asserted that Kuroiwa et al. "discloses the ruthenium silicide layer (conformal layer) 132 within an opening of the insulating film 110. The aspect ratio (ratio of height to width) is clearly greater than 1" (page 4, lines 13-15 of the Office Action mailed January 7, 2005). Applicants earnestly disagree with the Examiner's assertion.

For example, referring to Figure 3, Kuroiwa et al. disclose insulating film **110**, contact hole **110a**, and plug **111** (column 10, lines 41-42). Kuroiwa et al. further state that

> In the second embodiment, the plug **111** was made of polycrystal silicon containing doped phosphorus. To prevent oxidation of the plug **111** when the capacitor dielectric film **115** was formed, the polycrystal silicon was etched so that the top end of the plug **111** was made to be lower than the top surface of the first interlayer insulating film **110**. The preferred extent of lowering is 30 nm to 500 nm. In the second embodiment, it was determined to be 50 nm. A silicide layer **132** and the metal electrode **130** were formed to cover the plug **111** so as to serve as the lower electrode **114** of the capacitor. The material of the metal electrode **130** was ruthenium or iridium in place of platinum, which was the conventional material. By performing heat treatment at 600 ° C. or higher, a portion of the metal electrode **130** reacts with silicon in the plug **111** so as to be formed into the silicide layer **132**.

(Column 10, lines 48-63). Thus, Kuroiwa et al. disclose the formation of silicide layer 132 in the lowered top surface of insulating film 110 formed by etching plug 111. Applicants respectfully submit that nothing in this recitation or in Figure 3 would lead one of skill in the art to conclude that silicide layer 132 is formed in an opening having an aspect ration "clearly greater than 1" as suggested by the Examiner. In contrast, Figure 3 suggests that the opening formed by the lowered top surface of etched plug 111 has as aspect ratio less than 1.

Thus, for at least the reasons presented herein above, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness of claims 48, 49, and 54-68 under 35 U.S.C. §103.

Kuroiwa et al. in view of Aoyama et al., and in further view of Matsubara et al.

The Examiner rejected claims 52 and 53 under 35 U.S.C. §103 as being unpatentable over Kuroiwa et al. (U.S. Patent No. 6,239,460) in view of Aoyama et al. (U.S. Patent No. 5,852,307) and further in view of Matsubara et al. (U.S. Patent No. 5,122,923). Applicants respectfully traverse the rejection.

As discussed herein above, Kuroiwa et al. in view of Aoyama et al. fail to teach or suggest a chemical vapor deposited $RuSi_x$ diffusion barrier. Applicants respectfully submit that Matsubara et al., which has been discussed herein above in the traverse of the rejection under 35 U.S.C. §102, fail to cure the deficiencies of Kuroiwa et al. in view of Aoyama et al.

As such, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness of claims 52 and 53 under 35 U.S.C. §103.

Applicants respectfully request reconsideration and withdrawal of the rejections under 35 U.S.C. §103.

New Claims

New claims 69-74 are generally supported, for example, by claims 57-62, and further recite the proviso that the surface defining the opening is not a silicon containing surface (*see*, the Remarks section for illustrative support). Applicants note that claims 57-62 stand rejected only under 35 U.S.C. §103 as being unpatentable over Kuroiwa et al. in view of Aoyama et al. Applicants respectfully submit that new claims 69-74 are patentable over Kuroiwa et al. in view of Aoyama et al. for at least the reasons recited in the traverse of the rejection of claims 57-62 herein.

Further, Kuroiwa et al. disclose the deposition of ruthenium on a silicon plug, followed by heat treatment to form a ruthenium silicide layer through a salicidation process. Thus, the method disclosed by Kuroiwa et al. requires that the ruthenium be deposited on a silicon containing surface. In contrast, new claims 69-74 recite a chemical vapor codeposited diffusion barrier layer over at least a portion of a surface defining an opening, with the proviso that the

surface defining the opening is not a silicon containing surface. Thus, for at least the reasons recited herein, Applicants respectfully submit that new claims 69-74 are patentable over Kuroiwa et al. in view of Aoyama et al.

Entry and consideration of new claims 69-74 is respectfully requested.

Summary

It is respectfully submitted that all the pending claims are in condition for allowance and notification to that effect is respectfully requested. The Examiner is invited to contact Applicants' Representatives, at the below-listed telephone number, if it is believed that prosecution of this application may be assisted thereby.

Respectfully submitted for
Vaartstra et al.

By
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Customer Number 26813

May 9, 2005
Date

By: _____
Loren D. Albin
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Direct Dial (612) 305-1225

CERTIFICATE UNDER 37 CFR §1.8:
The undersigned hereby certifies that the the paper(s) are being transmitted by facsimile in accordance with 37 CFR §1.6(d) to the Patent and Trademark Office, addressed to **Mail Stop RCE**, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 9th day of May, 2005, at 1:55PM (Central Time).

By: _____
Name: Sara E. Olson

PATENT
Docket No. 150.00650102

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Vaartstra et al.	Group Art Unit:	2815
Serial No.:	09/603,132	Examiner:	Eugene Lee
Confirmation No.:	3538		
Filed:	June 23, 2000		

For: DEVICE STRUCTURES INCLUDING RUTHENIUM SILICIDE DIFFUSION BARRIER LAYERS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with C.F.R. §§ 1.97 *et. seq.*, the materials enclosed herewith are brought to the attention of the Examiner as possibly being of interest in connection with the above-identified patent application. Per M.P.E.P. § 609, the information cited in the present Information Disclosure Statement shall not be construed to be an admission that the information is, or is considered to be, material to patentability. Consideration of each of the documents listed on the attached 1449 form(s) is respectfully requested. Pursuant to the provisions of M.P.E.P. §609, Applicants further request that a copy of the 1449 form(s), marked as being considered and initialed by the Examiner, be returned with the next Official Communication.

It is believed that no fee is due, as this Information Disclosure Statement is filed prior to the receipt of any Action on the merits. However, in the event a fee is due, please charge any fee or credit any overpayment to Account No. 13-4895.

Supplemental Information Disclosure Statement
Applicant(s): Vaartstra et al.
Serial No.: 09/603,132
Confirmation No.: 3538
Filed: June 23, 2000
For: DEVICE STRUCTURES INCLUDING RUTHENIUM SILICIDE DIFFUSION BARRIER LAYERS

The Examiner is invited to contact Applicants' Representatives at the below-listed telephone number, if they can be of any assistance during prosecution of the present application.

Respectfully submitted for

Vaartstra et al.

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Customer Number 26813

CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper is being transmitted by facsimile in accordance with 37 CFR §1.6(d) to the Patent and Trademark Office, addressed to Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 9TH day of May, 2005, at 1:55pm (Central Time).

Name: Sara E. Olson

May 9, 2005
Date

By:
Loren D. Albin
Reg. No. 37,763
Direct Dial (612)305-1225

OMB No. 0651-0011
Page 1 of 2

INFORMATION DISCLOSURE STATEMENT	Atty. Docket No.: 150.00650102	Serial No.: 09/603,132
	Applicant(s): Vaartstra et al.	Confirmation No.: 3538
	Application Filing Date: June 23, 2000	Group: 2815
	Information Disclosure Statement mailed:	May 9, 2005

U.S. PATENT DOCUMENTS

Examiner Initial	Copy Enclosed	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
		5,962,716	10/05/99	Uhlenbrock et al.			
		6,074,945	06/13/00	Vaartstra et al.			
		6,114,557	09/05/00	Uhlenbrock et al.			
		6,133,159	10/17/00	Vaartstra et al.			
		6,197,628	03/06/01	Vaartstra et al.			
		6,204,172	03/20/01	Marsh			
		6,261,850	07/17/01	Marsh			
		6,281,125	08/28/01	Vaartstra et al.			
		6,284,655	09/04/01	Marsh			
		6,323,081	11/27/01	Marsh			
		6,323,511	11/27/01	Marsh			
		6,403,414	06/11/02	Marsh			
		6,429,127	08/06/02	Derderian et al.			
		6,455,423	09/24/02	Marsh			
		6,495,458	12/17/02	Marsh			
		6,576,778	06/10/03	Uhlenbrock et al.			
		6,784,504	08/31/04	Derderian et al.			
		6,872,420	03/29/05	Uhlenbrock et al.			
		2002/0008270	01/24/02	Marsh			
		2002/0058415	05/16/02	Derderian et al.			

EXAMINER	Date Considered

*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT	Atty. Docket No.: 150.00650102	Serial No.: 09/603,132
	Applicant(s): Vaartstra et al.	Confirmation No.: 3538
	Application Filing Date: June 23, 2000	Group: 2815
	Information Disclosure Statement mailed:	May 9, 2005

OTHER DOCUMENTS (Including Authors, Title, Date, Pertinent Papers, etc.)

Examiner Initial	Copy Enclosed	Document Description
	X	Wolf and Tauber, "Refractory Metals and Their Silicides in VLSI Fabrication," *Silicon Processing for the VLSI Era Volume 1: Process Technology*, Sunset Beach, California, 1986:384-393.
	X	Yang, "Types of Thin Film," *Thin Film Process*. [online]. [retrieved on 2005-05-03] from the Internet. Retrieved from the Internet:<URL:http://www-yiy.me.ntu.edu.tw/IC/6p.pdf: 11 pgs.

EXAMINER	Date Considered

*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Thin Film Process

Yao-Joe Yang

Ref: Campbell: Ch 12, 13, 14

Zant: Ch. 12

1

Types of Thin films

- Physical vapor deposition (PVD)
  - Evaporation
  - Sputtering
- Chemical vapor deposition (CVD)
  - LPCVD
  - PECVD
  - APCVD
- Epitaxial growth

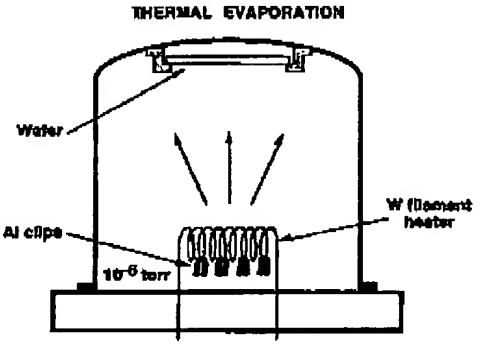
2

PVD

- Deposit film by physical methods
  - Thermal evaporation
    - Material source is heated to sublimation temperature in a vacuum
    - Material is vapor transported to target in vacuum
    - Deposition is by "line-of-sight" (mean free path = 50m)
  - Sputtering
    - Material is removed from target by momentum transfer
    - Gas molecules are ionized in a glow discharge, ions strike target and remove mainly neutral atoms
    - Atoms condense on the substrate
    - Vacuum level ~ 10 mtorr --> mean free path ~ 5 mm
    - Easy to deposit alloys

3

Evaporation



- Need high temperature
- Need high vacuum environment

4

Key Considerations of Evaporation

- Deposition rate
- Temperature
  - some metals requires excessive high temperature
- Contamination
- Step Coverage
  - an important issue in evaluating performance of deposition, usually poor in evaporation
- Residual stresses
  - usually due to mismatch of CTE and micro structures transformation

5

Step Coverage

- A primary limitation of evaporation
  - material beams are directional
- Need wafer rotation to improve step coverage
- Performance index
  - AR (step height/step diameter)
  - OK for AR < 0.5
  - marginal 0.5 < AR < 1
  - poor if AR >1

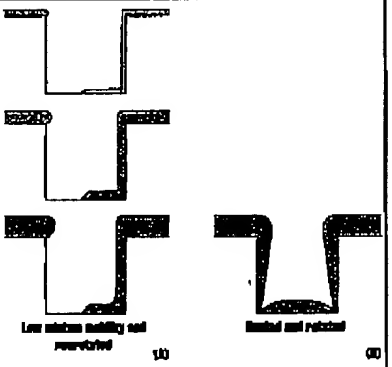
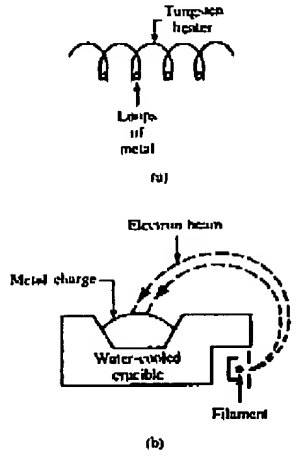


Figure 12-5 (a) Time evolution of the evaporative coating of a feature with aspect ratio of 1.0, with little surface atom mobility (i.e., low substrate temperature) and no rotation. (b) Final profile of deposition on rotated and heated substrates.

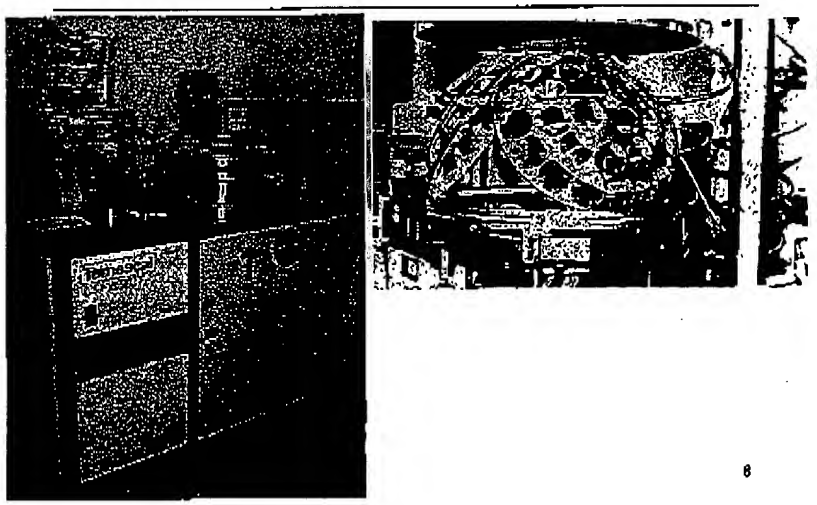
Type of Evaporation

- Filament evaporation
  - major problems
    - high contamination level
    - hard to form composite films
- Electron-beam evaporation
  - using high density electron beam to evaporate metals
  - dual E-beams with dual target can be used to co-evaporate composite materials
  - major problem: radiation damage for MOS devices (Campbell, p303)



7

Evaporator



8

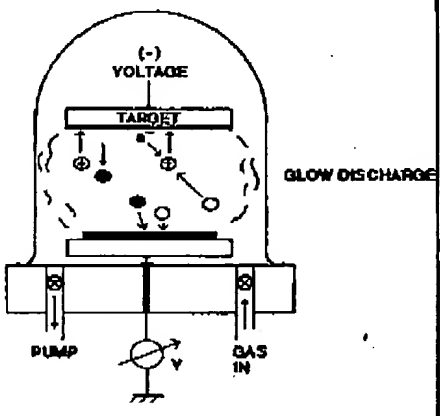
Sputtering

- The major PVD method in silicon technology
- Using ion bombardment to introduce mass transfer
- A low temperature process
  - can deposit virtually any materials, including metals, ceramics, and organic materials
  - can deposit composite film with controllable composition
- Substrate damage is the major disadvantage

9

Sputtering

- Argon (Ar) atoms is usually used as the ion source



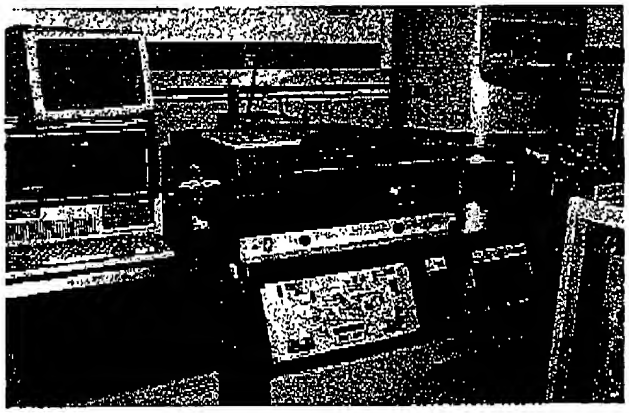
10

Sputtering vs. Evaporation

- Temperature
  - evaporation requires high temperature
- Materials
  - evaporation: metal only
  - sputtering: virtually any materials
- Sputtering has: (vs. evaporation)
  - better step coverage
  - less radiation damage
  - less contamination
  - more severe substrate damage

11

Sputter



12

Introduction to CVD

- Form thin films on the surface of a substrate by thermal decomposition and/or reaction of gaseous compounds
- Usually performed at high temperature
  - Can be performed at various pressure and with assistance of plasma
  - Usually at viscous flow regime

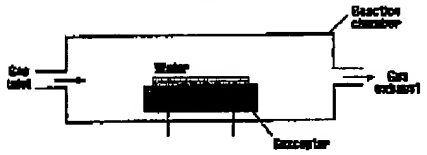


Figure 18-1 A simple prototype thermal CVD reactor.

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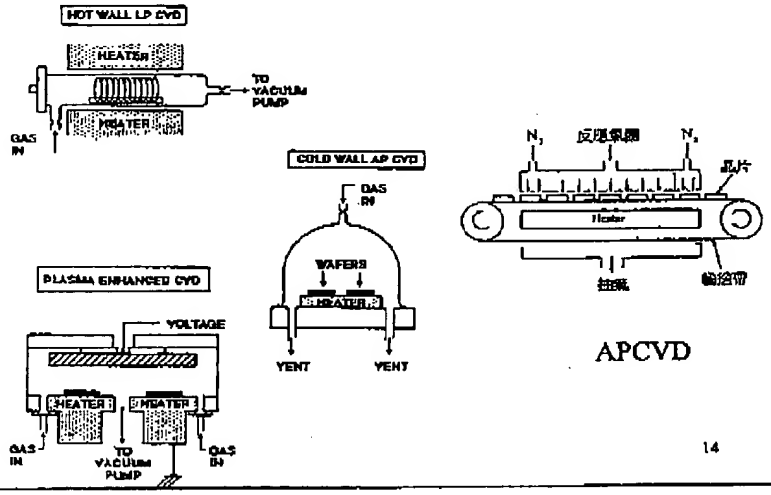
CVD Reaction Chambers



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Type of CVD

- APCVD
  - high deposition rate, poor uniformity, high contamination level, 250-450 °C
  - for dielectrics
- LPCVD
  - low deposition rate, high uniformity, 575-650 °C
  - for polysilicon
- PECVD
  - for extremely low deposition temperature
  - e.g, oxide and nitride
  - quality is poor

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Polysilicon

- Application:
  - gate of MOSFET, surface micromachining
- Usually deposited in a LPCVD chamber

$$SiH_4 \rightarrow (600^o C)\ Si + 2H_2$$

- Pressure: 25 - 150 KPa
- deposition rate ~ 0.01 - 0.02 μm/min
- Doping (Jaeger, p118)
  - In situ doping
    - Add dopant gases during deposition
  - thermal diffusion
    - performed right after deposition

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Silicon Nitride

- Application:
  - masks to prevent oxidation for LOCOS process
  - final passivation barrier for moisture and sodium contamination
- APCVD

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$$

- LPCVD

$$3SiCl_2H_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2$$

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Epitaxy

- Deposition of single crystal films on single crystal substrate
  - Vapor phase epitaxy (VPE)
    - For silicon process
    - Single silicon acts as a seed
  - liquid phase epitaxy (LPE) and molecular beam epitaxy (MBE)
    - For GaAs process
- To grow single crystal n-type layers on p-type substrates for bipolar processing
- Slow process

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CVD Vs. Epitaxy

- Crystalline
  - CVD: Polysilicon or amorphous
  - Epitaxy: single crystal
- Fluid dynamics
  - CVD: viscous flow regime
  - Epitaxy: molecular flow regime
- Technology
  - CVD: quite popular in Si technology
  - Epitaxy: mostly used in GaAs technology

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Thin Film Material Properties

- Chemical
  - in many situation, the composition is non-stoichiometric
- Material structures
  - columnar grain for polycrystalline materials
- Electrical
  - Conductivity/resistivity
  - Dielectric constant
  - breakdown voltage
- Mechanical
  - Dimension
  - Stiffness
  - residual stress

20

Residual Stress

- Residual stress
  - stress of the thin film under no external loading
  - A major mechanical problem in thin film materials
- Problem associated with residual stress
  - structural integrity
  - change of geometry, causing difficulty for subsequent processes
  - natural frequency shift of MEMS structures
- Major sources
  - mismatch in thermal mechanical properties
  - grain growth, impurity, phase transformation, etc

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SILICON PROCESSING FOR THE VLSI ERA

VOLUME 1:

PROCESS TECHNOLOGY

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REFRACTORY METALS and THEIR SILICIDES in VLSI FABRICATION

As the features of VLSI circuits continue to shrink to 1 μm (or less), the necessity of decreasing the resistance and capacitance (RC) associated with interconnection paths becomes ever more pressing. This is particularly true for MOS devices, in which the RC delay due to the interconnect paths can exceed the delays due to gate switching. The higher the value of the interconnect R (resistance) x C (capacitance) product, the more likely is the circuit operating speed to be limited by this delay. A simplified approach to the problem shows that:

$$RC = R_s L^2 \varepsilon_{ox} / x_{ox} \qquad (1)$$

where: R_s is the sheet resistance of the connection (given by, $R_s = \rho / x_{int}$); L is the length of the connection; x_{int} is the thickness of the interconnect conductor; x_{ox} is the oxide thickness over which the connection runs; and ε_{ox} is the permittivity of SiO_2. In reducing x_{ox} and x_{int}, RC depends only on L, and not the width of the conductor, W. This simple model however, is inaccurate for W<3 μm, where capacitance fringing-fields become important. Since the R_s decreases with decreasing line size, the RC product also decreases. Figure 1 shows the RC time constant for a 1 cm line as a function of design rule for polysilicon, tantalum silicide ($TaSi_2$), and aluminum (Al). Shown for comparison is the gate delay per stage for a MOS device. For small feature sizes, the interconnect delay could predominate, depending on the maximum length of the interconnect lines in the circuit. *The conclusion is that low resistivity interconnection paths are critical in order to fabricate dense, high performance devices*[1].

There are several potential approaches to reduce the resistivity of the interconnect to less than the 15-30 Ω /sq exhibited by polysilicon. The poly-Si could be replaced by Al, but due to the low melting and eutectic temperatures of Al, all subsequent processes would have to be held to less than 500°C. Since several post-gate formation processes must be carried out at temperatures >500°C (e.g. source-drain implant anneals, oxidation, and glass flow /reflow), Al is not a suitable alternative material. The poly-Si could also be replaced by a refractory metal (e.g. W, Ta, or Mo), a refractory metal silicide (e.g. WSi_2, $TiSi_2$, $MoSi_2$, or $TaSi_2$), or a multilayer structure, consisting of a low resistance material (e.g. a refractory metal silicide) on top of a doped polysilicon layer (such a structure is termed a *polycide*). Figure 1a shows a polycide configuration. The refractory metals have adequately high melting temperatures, but their oxides are typically of poor quality, and in some cases volatile (e.g. Mo and W oxides). In addition, it may be difficult to obtain consistent threshold voltages in MOS transistors due to

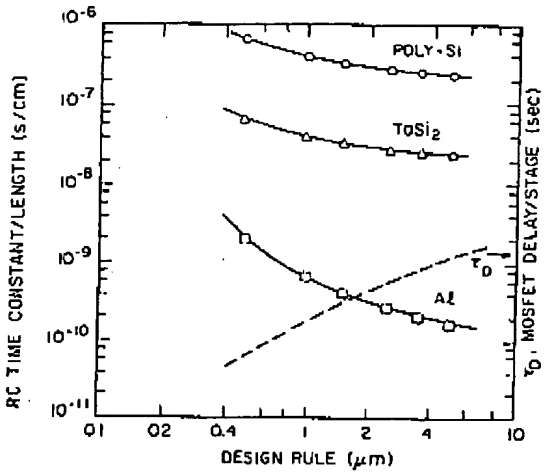


Fig. 1 RC time constant per unit length for three conductive materials as a function of feature size. Also shown is delay per stage of ring oscillators as a function of feature size. (After Sinha[1]) Reprinted with permission of American Physical Society.

impurities in the sources of the refractory metals. Use of refractory metal silicides alone as the gate /interconnect layer, suffers similar problems as those associated with the use of refractory metals alone. The *polycide* structure has therefore become the predominant gate /interconnect film for replacing polysilicon. In this way, the advantages of the known work function of poly-Si and the highly reliable poly-Si /SiO_2 interface are preserved, as poly-Si is still directly atop the gate oxide. In addition, the poly-Si provides a source of silicon for oxidation, and thereby allows isolation oxides for subsequent poly-Si or metal layers to be formed on the silicide.

Numerous studies on the preparation and properties of silicides, particularly using the polycide structure, have been published, and are surveyed in extensive detail in a comprehensive book by Murarka[2]. The major emphasis of this chapter is to present a brief overview of the

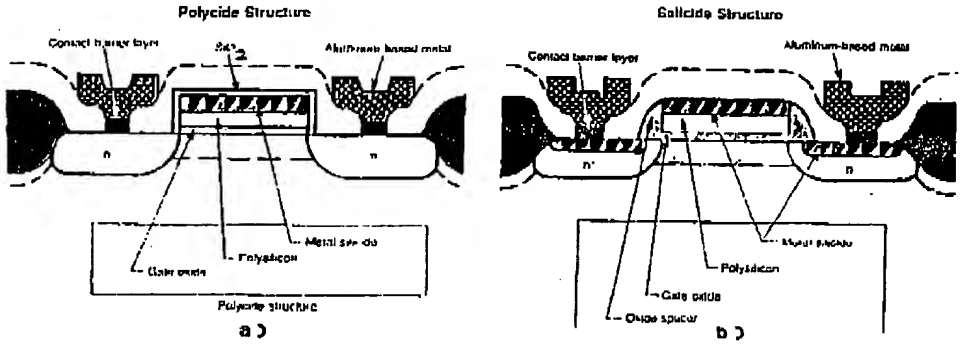


Fig. 2 (a) Polycide, and (b) Salicide structure. Reprinted by permission Semiconductor Internatl.

Table 1. SILICIDE MATERIAL PROPERTY REQUIREMENTS FOR VLSI[2]

- Low Electrical Resistivity
- Ease of Formation
- Ease of Fine Line Pattern Transfer
- Controlled Oxidation Properties and Stability in an Oxidizing Ambient
- High Temperature Stability
- Smooth Surface Features
- Good Corrosion Resistance
- Stable Contact Formation to Aluminum Metallization
- Excellent Adhesion and Low Stress
- Good Electromigration Resistance
- Ohmic and Low Contact Resistance
- Stability throughout Subsequent high-temperature Processing, including Ion Implant and Diffusion

properties and preparation of silicides and refractory metals for VLSI applications, including some new data that has been reported since the time Murarka's text was published.

CANDIDATE SILICIDES FOR VLSI APPLICATIONS

In order to effectively utilize refractory metal silicides in VLSI fabrication (either alone, or in the polycide configuration), very stringent materials requirements must be satisfied. Table 1 lists some of the most important of these requirements.

There are a group of refractory metal silicides (MSi_x) that meet most, or all of these criteria. For example, the refractory metal silicides can withstand much higher temperatures than aluminum, and their eutectic temperatures with Si are in excess of 1300°C. On the other hand, the silicides of Pd (Pd_2Si), Pt (PtSi), and Ni ($NiSi_2$), have eutectic temperatures of 720°C, 830°C, and 966°C, respectively. Hence these three silicides are not suitable for processes in which they are subjected to temperatures that approach their silicide-Si eutectic temperature.

Resistivity

Resistivity is the key parameter of a silicide that reduces interconnect delay, and Table 2 lists the resistivities of the most commonly used silicides. The resistivity values quoted in the Table 2 are for specific annealing times and temperatures. The resistivity values depend on many factors, including the method of formation, the sintering time and temperature, the stoichiometry of the compound, and its chemical purity. Table 2 clearly points out the significant differences between the materials that depend upon the method used to form them. It

Table 2. Resistivity of Silicide Films Annealed at ≤1000°C (in μΩ-cm).

Material	Metal + Poly-Si	Metal + Si Crystal	Co-Sputter	Co-Evaporation	CVD
$TiSi_2$	13	15	25	21	21
$TaSi_2$	35		50		38
$MoSi_2$	90	15	100	40	120
WSi_2			70	30	40
PtSi	28		35		

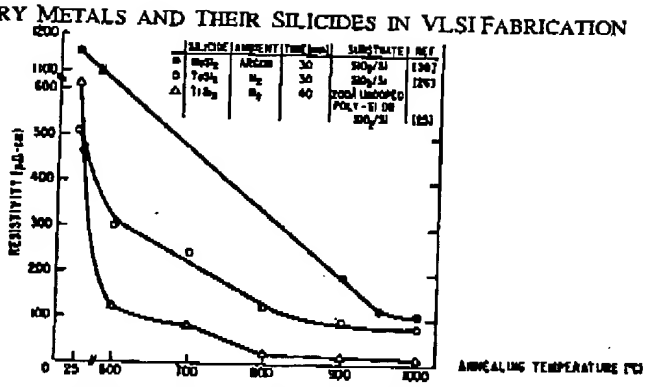


Fig. 3 Sheet resistivity of metal silicide ($MoSi_2$, $TaSi_2$, $TiSi_2$) films versus annealing temperature[3]. (© 1983 IEEE.)

should be noted that the lowest resistivity of the group (~13 μΩ-cm) is achieved by $TiSi_2$ formed by direct metallurgical reaction.

Figure 3 shows the resistivity of $MoSi_2$, $TaSi_2$, and $TiSi_2$ as a function of *annealing temperature*[3]. $TiSi_2$ achieves its minimum resistivity at 800°C, while $MoSi_2$ requires temperatures in excess of 900°C[3]. Figure 4 shows the effect of *annealing time* on the sheet resistance for several silicides. In all cases, equilibrium is achieved in less than 30 minutes. The use of rapid thermal processing (RTP), as described in Chap. 2, allows reaction times for WSi_2 formation to be under 60 sec at 1200°C[4].

The resistivity dependence on *stoichiometry* can be illustrated with a few examples. The resistivity of chemically vapor deposited WSi_x is shown in Fig. 5, where x varies from 2.2 to 2.6. The resistivity of the film increases as it becomes progressively richer in Si. Figure 6 shows the resistivity of co-sputtered $TiSi_2$ films as a function of Si /Ti ratio before and after sintering (900°C /30 min). The resistivity of the unsintered material increases with increasing Si content. For sintered films, however, the resistivity goes through a minimum at Si /Ti = 3 (nominal atomic ratio). $TiSi_2$ is formed only where the ratio exceeds 2. The resistivity decreases

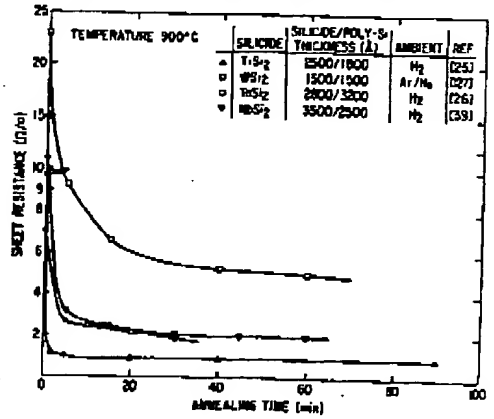


Fig. 4 Sheet resistance of polycide (WSi_2, $NbSi_2$, $TiSi_2$) films versus annealing time. (© 1983 IEEE.)

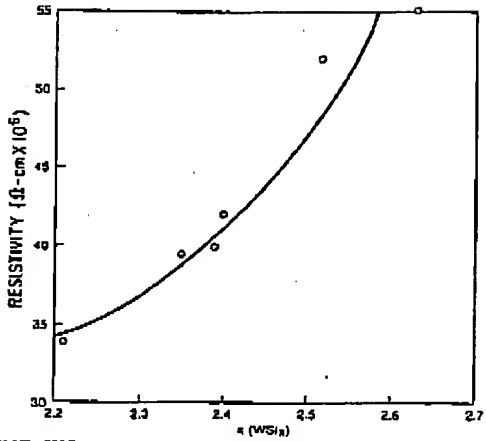


Fig. 5 Resistivity of CVD WSi_x versus x, where x varies from 2.2 to 2.6.Courtesy of Genus Inc.

for $TiSi_2$ with excess Si up to a value of Si /Ti = 5 /2, and then increases at higher Si content as the Si may undergo precipitation[6] (exact composition is determined by RBS, see Chap. 17).

Oxygen contamination in the silicide film also has a significant effect on the film resistivity. Figure 7 shows the effect of oxygen in as-deposited and sintered 2500Å thick $TaSi_2$ films. The sintering conditions were 900°C for 30 min in argon[3].

SILICIDE FORMATION

The silicides of interest can be formed by basically three techniques, each of which involve a deposition followed by a thermal step to form the silicide: 1) deposition of the pure metal on

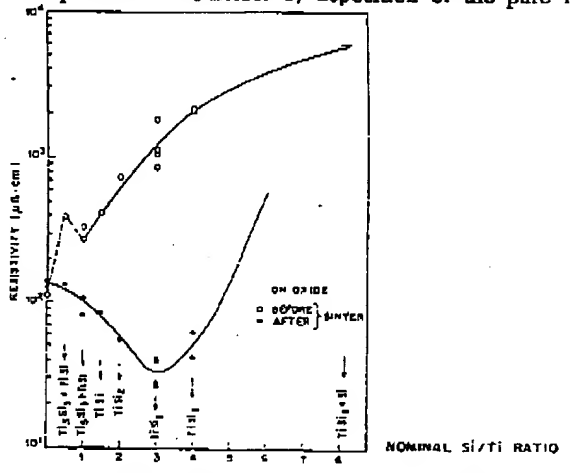


Fig. 6 Resistivity of cosputtered films on SiO_2 before & after sintering at 900°C for 30 min in H_2 as function of nominal Si /Ti ratio in film[6]. Reprinted with permission of American Phys. Soc.

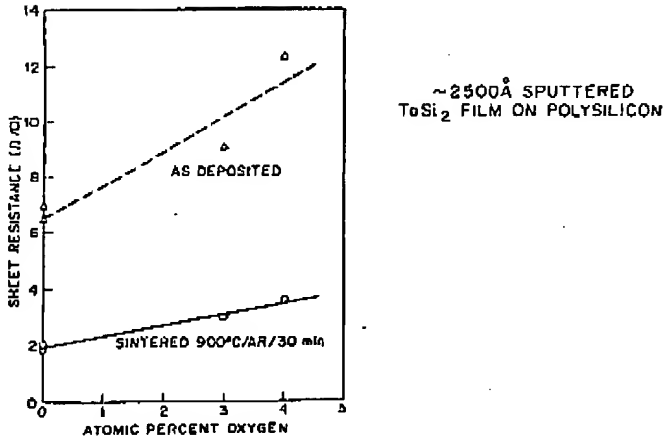


Fig. 7 Sheet resistance of the as-deposited and sintered cosputtered $TaSi_2$ films as a function of the oxygen concentration in the film[2]. Reprinted with permission of American Physical Society.

silicon (i.e. onto single crystal and /or polycrystalline Si); 2) simultaneous evaporation of the silicon and the refractory metal from two sources (co-evaporation); and 3) sputter-depositing the silicide, either from a composite target, or by co-sputtering or layering. Table 3 lists the methods of formation and some of the advantages and disadvantages of each.

Table 3. METHODS OF SILICIDE FORMATION

Method of Formation	Advantages	Disadvantages
Direct Metallurgical Reaction. $M + xSi \Rightarrow MSi_x$ Metal deposited by evaporation, sputter, or CVD.	Both polycide and salicide structure can be formed. Selective etch possible.	[M] /[Si] depends on phase formed. Sensitive to sintering environment. Rough surface.
Co-evaporation from an Independent Si and M Source.	Smooth surface. Sintering environment not as critical	[M] /[Si] control difficult but possible. No selective etch possible. Poor step coverage.
Co-sputtering from Independent Si and M Targets.	Good control of [M] /[Si]. Smooth films. Sintering environment not as critical. Deposition of sandwich possible.	Difficult calibration to achieve [M] /[Si] control.
Sputtering from a Composite MSi_x Target.	Excellent [M] /[Si] control if correct target chosen. Good step coverage.	Contamination from Target.
Chemical Vapor Deposition: atmospheric, low-pressure, or plasma-enhanced.	High throughput. Excellent step coverage.	Rough surface. [M] /[Si] control difficult but possible. Possible poor adhesion.

Direct Metallurgical Reaction

When a refractory metal film is deposited directly on a silicon surface, and the wafer is subjected to heating, the metal and the silicon can react to form a silicide. One advantage of this method of silicide formation is that it usually yields a lower resistivity than most other methods. A significant body of work has been published on the formation and kinetics of such intermetallic compounds of thin film metals and silicon, both for single-crystal and polycrystalline silicon. Specialized techniques including RBS, AES, XPS, SIMS, and electrical measurements, have been used to follow the phase formations as the reactions proceed. See Chap. 17 for additional information on the analytical techniques.

For a metal film deposited on silicon, and annealed at relatively low temperatures, *metal-rich* silicides form first, and continue to grow until the metal is consumed. Typically, at that point, the next *silicon-rich* phase begins to grow. For example, Fig. 8 shows the effect of temperature on the formation of TiSi and $TiSi_2$. Above 600°C, no evidence of $TiSi_2$ exists, while TiSi begins to grow. The growth of TiSi peaks at 700°C, and the compound is not stable above 800°C. $TiSi_2$ begins to grow at 600°C, reaching a maximum at 800°C, and no more polysilicon is consumed above this temperature. After the complete conversion to $TiSi_2$, the system is stable. At 700°C it takes approximately 60 minutes until the $TiSi_2$ has completely formed, while no silicide is detected even after 10 hours at 500°C.

The Pt /Si reaction proceeds at 350°C. RBS studies on a sample sintered for 20 min shows that it is converted to Pt_2Si, with small amounts of PtSI present. After 60 minutes, nearly 65% of the Pt_2Si film is converted to PtSi. Canali[9] analyzed the time dependence of the Pt silicide formation, and found that the layer thickness x, is given by:

$$x^2_{Pt_2Si} = D_1 t \quad (2)$$

$$x^2_{PtSi} = D_2 (t - t_0) \quad (3)$$

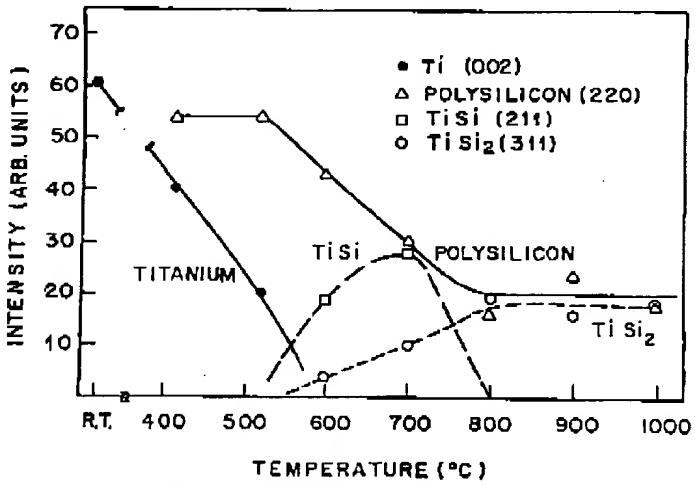


Fig. 8 X-ray diffraction intensities (integrated) of titanium, polysilicon, TiSi and $TiSi_2$ as a function of vacuum sintering temperature[8]. Reprinted with permission of American Physical Society.

where D_1 and D_2 are the interface diffusivities for Pt_2Si and PtSi, respectively, and t_0 is the time at which PtSi starts forming. Plots of D_1 and D_2 versus reciprocal temperature show an Arrhenius behavior (see Appendix 4), which yields activation energies of 1.3 and 1.5 eV for Pt_2Si and PtSi formation, respectively.

The $t^{1/2}$ dependence, which has been observed for most silicide formation, is indicative of a diffusion-limited process. The linear dependence, as seen during the formation of some other silicides, is indicative of a surface-reaction rate-controlled process. Difficulty in interpreting the reaction data results from the variation in the cleanliness of the interface, which has the effect of preventing the initiation of the reaction.

When a silicide is formed by direct reaction, silicon is consumed. For example in the WSi_2 reaction, for each angstrom of tungsten thickness consumed, 2.53Å of silicon are consumed, resulting in 2.58Å of WSi_2 being formed. Care must be exercised that sufficient silicon is available when using this technique.

Co-Evaporation

The evaporation method utilizes the simultaneous deposition of the metal and the Si under high vacuum conditions. The metal and silicon can be vaporized by electron beam, rf induction, laser, or resistive heating. Since the refractory metals (i.e. Ti, Ta, Mo, W) have very high melting points (1670°C to 2996°C), and silicon has a low vapor pressure, e-beam evaporation is the technique of choice (see Chap. 10). Typically, two guns are employed with separate power supplies. Careful determination of the evaporation rate as a function of power for both metal and Si must be determined. The correct amount of power is supplied to each gun to provide the proper (M /Si) ratio. X-ray damage from e-beam evaporation is generally annealed out during the high temperature sinter operation. In addition, the gate oxide is typically protected by polysilicon during the evaporation, which prevents radiation damage of the gate oxide. Careful control of the evaporation base pressure ($<10^{-6}$ torr), evaporation rates, purity of the elements, and residual gases in the vacuum chamber are critical to insuring that films with reproducible characteristics are deposited. The as-deposited resistivity and thickness should be monitored, and the (metal /Si) ratio measured by analytical techniques, as discussed in Chap. 17.

The very high temperatures needed to evaporate the refractory metals puts stringent requirements on the vacuum systems, and causes much higher susceptiblity to contamination due to outgassing. For example, to obtain a vapor pressure of 10^{-2} torr, Ti, Mo, Ta, and W must be heated to 1700°C, 2500°C, 3100°C, and 3200°C, respectively. Thus it appears that only $TiSi_2$ is likely to be satisfactorily deposited by co-evaporation in a manufacturing environment[10] (although $MoSi_2$, $TaSi_2$, and WSi_2 have all reportedly been successfully deposited by co-evaporation in research laboratories[4,11,12]).

Sputter Deposition: Co-Sputtering and Sputtering from Composite Targets

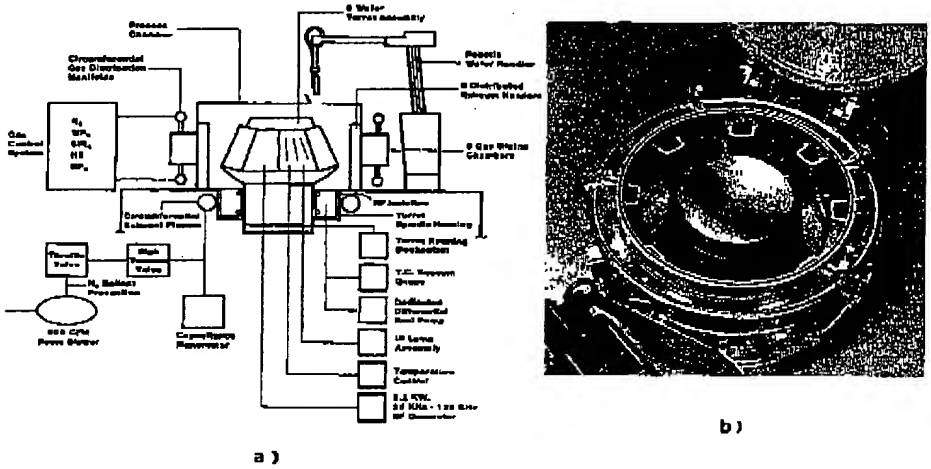
Sputtering is an excellent method for preparation of silicides. Both rf and magnetron sputtering can be employed (see Chap. 10). As in co-evaporation, the sputtering rates of the metal and the Si must be carefully established. Sputtering can be done in older-style sputtering systems from two "S" type guns (see Chap. 10) onto wafers mounted on a planetary. Care must be exercised to maintain the gun stability during the processing. Sputtering from two targets in more recently designed multi-pass sputtering systems can also achieve an appropriate mixture of Si and metal, resulting in a layered structure. After sintering, complete reaction between metal

and Si occurs, forming the silicide. As described in Chap. 10, the base pressure of the sputtering system should be lower than 10^{-6} torr, to minimize incorporation of residual gases during deposition. In the newer sputtering systems the short distance between the target and substrate allows high deposition rates, and therefore shorter deposition times, resulting in lower concentrations of included residual gases. The step coverage of co-sputtered films is also superior to that of evaporated films, and can be further improved by applying dc bias to the substrate. The bias also results in changes in surface texture (generally rougher), and increased residual gas incorporation and film stress.

Sputtering from a composite target (MSi_x) would appear to be ideal for compositional control and desired stoichiometry. Composite targets for silicide deposition, however, are usually manufactured by powder metallurgical techniques, which employ a mixture of fine particles of metal and Si. The powders are pressed together, and sintered at high temperatures and pressures, to 70-80% of their theoretical density. This fabrication process may result in sodium contamination of the targets. Improvements have been made to these processes, so that targets are available with low levels of contamination. Resistivities of silicide films comparable to those achieved with co-evaporation have been reported. In general, targets with varying ratios of (metal /Si) must be purchased to achieve the optimum stoichiometry in the deposited film. Care must be exercised to insure the sputtering yields of the metal and Si remain equal, otherwise compositional changes will occur over time. Reference 10 compares the properties of co-sputtered and layered sputter-deposited silicides, and reports that both deposition methods are capable of producing good quality silicide films. Reference 3 is another source that describes the properties of various sputtered silicide films.

Chemical Vapor Deposition (CVD) of Silicides

CVD offers several advantages over other techniques for silicide formation including, improved step coverage, higher purity films (low O_2 content), and higher throughput. In order to use CVD techniques, volatile components of the metal must exist. Considerable effort has been



a) b)

Fig. 9 (a) Schematic of cold-wall reactor for CVD of WSi_2 and W. (b) Photograph of system. Courtesy of Genus Inc.